UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,762	12/29/2000	Sailesh Kottapalli	2207/10121	5066

7590 12/22/2003

Kenyon & Kenyon
Suite 600
333 W. San Carlos Street
San Jose, CA 95110-2711

EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 12/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,762	KOTTAPALLI ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *06 April 2001 and 07 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Received

2. Receipt is acknowledged of Declaration and Formal Drawings papers submitted, where the papers have been placed of record in the file.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method for Converting Pipeline Stalls Caused by Instructions with Long Latency Memory Accesses to Pipeline Flushes in a Multithreaded Processor Where the Instructions are Re-executed Upon Completion of the Accesses.

4. The disclosure is objected to because of the following informalities: the specification does not contain a summary of the invention. See MPEP § 1.73.

Appropriate correction is required.

Claim Objections

5. Claim 1 is objected to because of the following informalities: line 1 states the word "operation" when the correct term is the plural, "operations".

6. Claim 10 is objected to because of the following informalities: line 2 states: "from first thread and second threads". The examiner is taking this statement to mean its proper grammatical form: "from a first thread and a second thread".

7. Claim 16 is objected to because of the following informalities: line 4 states: "from first thread and second threads". The examiner is taking this statement to mean its proper grammatical form: "from a first thread and a second thread".

8. Claim 18 is objected to because of the following informalities: the claim refers back to claim 10 as its parent claim, which is the previous independent claim. The preamble of claim 18 as being a computing system does not correctly match the parent claim 10, which is a processing system. The examiner is taking the claim to have its parent actually be claim 16 instead of 10 in order to be consistent and resolve any scope issues.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 10-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 10 recites the limitation "a first thread" in line 5. There is insufficient antecedent basis for this limitation in the claim. Line 2 has already defined a first thread so it is unclear whether the first thread of mention in line 5 is referring to the same thread or a different one. The examiner is taking the phrase of line 5 to mean "said first thread" based on the specification.

12. Claim 16 recites the limitation "a first thread" in line 7. There is insufficient antecedent basis for this limitation in the claim. Line 4 has already defined a first thread so it is unclear whether the first thread of mention in line 7 is referring to the same thread or a different one. The examiner is taking the phrase of line 7 to mean "said first thread" based on the specification.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-21 rejected under 35 U.S.C. 102(b) as being anticipated by Parady (5,933,627).

15. In regard to claim 1, Parady discloses a method of handling operations in a multi-threaded processing system (figures 1 and 3), comprising:

a. determining if a stalled operation of a first thread is due to a loading of data from a memory device; Column 4, lines 57-59, show that blocking loads exist, which stall the operation on a memory access. Column 4, lines 59-62 then show that a thread switch occurs on this blocking load waiting for data.

b. and flushing an instruction from said first thread from a pipeline of said processing system when data is to be loaded from said memory device before executing said instruction. As shown above, the system switches threads when data is to be loaded from said memory device before executing said instruction.

Column 4, lines 42-48 show that the thread with the memory access instruction is later re-executed once scheduled. This means that the instruction did not finish execution when the thread switch occurred and must have been flushed.

16. In regard to claim 2, Parady discloses the method of claim 1, as described above, wherein said memory device is system memory coupled to a memory bus. Column 3, lines 58-61 show that a case for thread switching that involves a memory access would be when an L2 cache (figure 2, elements 80 and 82) misses. It is inherent that upon an L2 cache miss, data must be loaded from main memory. Figure 2 shows a memory bus, 86, that is coupled to main memory (system memory) that is used for getting data on a cache miss.

17. In regard to claim 3, Parady discloses the method of claim 1, as described above, further comprising: marking said instruction as a miss. Column 3, lines 58-61 show that a case for thread switching that involves a memory access would be when an L2 cache (figure 2, elements 80 and 82) misses. Thus the instruction is marked as a miss so the data can be retrieved from main memory.

18. In regard to claim 4, Parady discloses the method of claim 3, as described above, further comprising: rescheduling said instruction to be executed in said pipeline. Column 4, lines 42-48 show that the thread and the instruction causing the switch is rescheduled for execution.

19. In regard to claim 5, Parady discloses a method of handling operations in a multi-threaded processing system (figures 1 and 3), comprising:

c. determining if a stalled operation of a first thread is due to a loading of data from a memory device; Column 4, lines 57-59, show that blocking loads exist, which stall the operation on a memory access. Column 4, lines 59-62 then show that a thread switch occurs on this blocking load waiting for data.

d. and flushing an instruction from said first thread from a pipeline of said processing system when data is to be loaded after a predetermined number of clock cycles from said memory device before executing said instruction. As shown above, the system switches threads when data is to be loaded from said memory device before executing said instruction. Column 4, lines 42-48 show that the thread with the memory access instruction is later re-executed once scheduled. This means that the instruction did not finish execution when the thread switch occurred and must have been flushed. Since a predetermined number of clock cycles is not further defined and could be any number, one can apply zero to be the predetermined number of clock cycles. Therefore, the flushing is performed when data is to be loaded after a predetermined number of clock cycles from memory.

20. In regard to claim 6, Parady discloses the method of claim 5, as described above, wherein said memory device is system memory coupled to a memory bus. Column 3, lines 58-61 show that a case for thread switching that involves a memory access would be when an L2 cache (figure 2, elements 80 and 82) misses. It is inherent that upon an L2 cache miss, data must be loaded from main memory. Figure 2

shows a memory bus, 86, that is coupled to main memory (system memory) that is used for getting data on a cache miss.

21. In regard to claim 7, Parady discloses the method of claim 6, as described above, further comprising: marking said instruction as a miss. Column 3, lines 58-61 show that a case for thread switching that involves a memory access would be when an L2 cache (figure 2, elements 80 and 82) misses. Thus the instruction is marked as a miss so the data can be retrieved from main memory.

22. In regard to claim 8, Parady discloses the method of claim 7, as described above, further comprising: rescheduling said instruction to be executed in said pipeline. Column 4, lines 42-48 show that the thread and the instruction causing the switch are rescheduled for execution.

23. In regard to claim 9, Parady discloses the method of claim 8, as described above, further comprising: executing said instruction when data is loaded from said memory device. Column 4, lines 42-48 show that a thread (and its stalled instruction) can be restarted as soon as the memory access is complete.

24. In regard to claim 10, Parady discloses a processing system comprising:

a. a scheduler to pass instructions from a first thread and a second thread to an execution pipeline (figure 3, element 28);

b. and pipeline control logic (figure 3, element 112 and figure 1, element 22) coupled to said execution pipeline to determine if a stalled execution of a first thread is due to a loading of data from a memory device and to flush an instruction from said first thread from said execution pipeline when data is to be

loaded from said memory device before said instruction can be executed. Column 4, lines 57-59, show that blocking loads exist, which stall the operation on a memory access. Column 4, lines 59-62 then show that a thread switch occurs on this blocking load waiting for data. Column 4, lines 42-48 show that the thread with the memory access instruction is later re-executed once scheduled. This means that the instruction did not finish execution when the thread switch occurred and must have been flushed. Column 3, lines 58-61 show that a case for thread switching that involves a memory access would be when an L2 cache (figure 2, elements 80 and 82) misses. It is inherent that upon an L2 cache miss data must be loaded from main memory. The thread switch logic will receive a signal from the cache showing a cache miss, as shown in figure 3, to show that a memory access is required and the thread switch logic will then carry out the flush.

25. In regard to claim 11, Parady discloses the processing system of claim 10, as described above, wherein said pipeline control logic is to mark said instruction as a miss. As shown above, the pipeline control logic includes the cache control. Thus on a cache miss the instruction will be marked as a miss by the pipeline control logic.

26. In regard to claim 12, Parady discloses the processing system of claim 10, as described above, further comprising: an exception and retirement logic (figure 3, element 112) coupled to said execution pipeline.

27. In regard to claim 13, Parady discloses the processing system of claim 12, as described above, wherein said instruction marked as a miss is to be detected by said

exception and retirement logic. As shown above, the pipeline control logic includes the cache control. Thus on a cache miss the instruction will be marked as a miss by the pipeline control logic. Also as shown above, the thread switching logic, receives this cache miss signal, or detects it. Thus the exception and retirement logic detects the instruction marked as a miss.

28. In regard to claim 14, Parady discloses the processing system of claim 13, as described above, further comprising: a fetch unit (figure 1, element 16) to provide said instruction to said scheduler.

29. In regard to claim 15, Parady discloses the processing system of claim 14, as described above, wherein said pipeline control logic is to cause said instruction to be executed when data is loaded from said memory device. Column 4, lines 42-48 show that a thread (and its stalled instruction) can be restarted as soon as the memory access is complete. Column 3, lines 54-56 shows that the threads pick up where left off upon the switch. Thus the thread control logic and further the pipeline control logic must be in control of the event.

30. In regard to claim 16, Parady discloses a computing system comprising:

a. a memory bus (figure 3, element 114) coupled to system memory;

b. and a processing system (figures 3 and 1) coupled to said memory bus, said processing system including

i. a scheduler (figure 3, element 28) to pass instructions from first thread and second threads to an execution pipeline;

ii. and pipeline control logic (figure 3, element 112 and figure 1, element 22) coupled to said execution pipeline to determine if a stalled execution of a first thread is due to a loading of data from system memory and to flush an instruction from said first thread from said execution pipeline when data is to be loaded from said system memory before said instruction can be executed. Column 4, lines 57-59, show that blocking loads exist, which stall the operation on a memory access. Column 4, lines 59-62 then show that a thread switch occurs on this blocking load waiting for data. Column 4, lines 42-48 show that the thread with the memory access instruction is later re-executed once scheduled. This means that the instruction did not finish execution when the thread switch occurred and must have been flushed. Column 3, lines 58-61 show that a case for thread switching that involves a memory access would be when an L2 cache (figure 2, elements 80 and 82) misses. It is inherent that upon an L2 cache miss data must be loaded from main memory. The thread switch logic will receive a signal from the cache showing a cache miss, as shown in figure 3, to show that a memory access is required and the thread switch logic will then carry out the flush.

31. In regard to claim 17, Parady discloses the computing system of claim 16, as described above, wherein said pipeline control logic is to mark said instruction as a miss. As shown above, the pipeline control logic includes the cache control. Thus on a cache miss the instruction will be marked as a miss by the pipeline control logic.

32. In regard to claim 18, Parady discloses the computing system of claim 16 wherein said processing system further includes an exception and retirement logic (figure 3, element 112) coupled to said execution pipeline.

33. In regard to claim 19, Parady discloses the computing system of claim 18, as described above, wherein said instruction marked as a miss is to be detected by said exception and retirement logic. As shown above, the pipeline control logic includes the cache control. Thus on a cache miss the instruction will be marked as a miss by the pipeline control logic. Also as shown above, the thread switching logic, receives this cache miss signal, or detects it. Thus the exception and retirement logic detects the instruction marked as a miss.

34. In regard to claim 20, Parady discloses the computing system of claim 19, as described above, wherein said processing system further includes a fetch unit (figure 1, element 16) to provide said instruction to said scheduler.

35. In regard to claim 21, Parady discloses the computing system of claim 20, as described above, wherein said pipeline control logic is to cause said instruction to be executed when data is loaded from said system memory. Column 4, lines 42-48 show that a thread (and its stalled instruction) can be restarted as soon as the memory access is complete. Column 3, lines 54-56 shows that the threads pick up where left off upon the switch. Thus the thread control logic and further the pipeline control logic must be in control of the event.

Conclusion

36. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to multithreaded flushing and switching.

US Pat No 5,361,337 to Okin shows a method and apparatus for switching threads on a cache miss which leads to loading data from memory.

US Pat No 5,553,305 to Gregor shows a multithreaded system that sets aside a thread with an instruction waiting for a memory access and then places it back in the execute buffer when the memory access is finished.

US Pat No 6,016,542 to Gottlieb shows means for detecting long latency pipeline stalls for thread switching where the current thread is flushed from the pipeline.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
December 10, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER